Fine Pitch Cu Pillar with Bond on Lead (BOL) Assembly Challenges for Low Cost and High Performance Flip Chip Package

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Abstract

Fine pitch copper (Cu) pillar bump adoption has been growing in high performance and low-cost flip chip packages. Higher input/output (I/O) density and very fine pitch requirements are driving very small feature sizes such as small bump on a narrow pad or bond-on-lead (BOL) interconnection, while higher performance requirements are driving increased current densities. Assembling such packages using a standard mass reflow (MR) process and maintaining its performance is a real and serious challenge. Typical thermal compression bonding (TCB) using non-conductive paste can be used to mitigate the assembly risk up to a certain extent of die size and package body size. On the other hand, the TCB process results in a significantly higher assembly cost due to very low throughput. The very cost sensitive consumer market is not quite ready to adopt TCB process for this reason. To address the need for fine pitch Cu pillar flip chip, a technology featuring copper pillar Bond-On-Lead (BOL) with enhanced processes, known as fcCuBE®, delivers the cost effective, high performance packaging solution that is required by the industry. BOL substrate technology with standard MR is becoming popular for high performance flip chip BGA (fcBGA) assembly. fcCuBE® technology provides an extended roadmap to very fine pitches (less than 100 um) for fcBGA packages which are not available in conventional mass reflow interconnect technologies. There are some published papers that have addressed BOL or similar types of technology on small body size flip chip CSP type packages. However, none of the literature truly addresses the assembly challenges and risk mitigation plan for bigger body size fine pitch fcBGA packages. fcCuBE provides added benefits of cost reduction through elimination of Solder on Pad (SOP) in the substrate as well as substrate layer reduction for fcBGA packages. Additionally, fcCuBE technology in a fcBGA package can drive higher I/O density, enabling advanced silicon (Si) nodes and die shrink which can further reduce the silicon cost due to an increased number of dies per wafer. In this study a comprehensive finding on the assembly challenges, package design, and reliability, and cost data for fcBGA packages will be published.

Keywords: flip chip, fine pitch, Cu pillar, BOL, fcBGA

Introduction

In consumer applications such as set top boxes (STB) and digital television (DTV) integrated ciruits (ICs), higher functionality, faster data rates and increased bandwidth are required for enhanced user interfaces, rich graphics and outstanding audio quality. Wire bonding technology, a popular packaging choice in the past, is often unable to successfully address the increased thermal and electrical performance requirements for next generation consumer applications and, as a result, semiconductor companies are turning to high performance flip chip interconnect to differentiate their products. The BOL interconnection and very fine pitch Cu bumps in fcCuBE® technology deliver exceptionally high I/O density and bandwidth with excellent electromigration (EM) performance for high current carrying applications such as STB and DTV ICs at a cost competitive price in the industry.

The functional and performance requirements for other application areas such as networking and communication continue to evolve as well, driving demand for larger and thinner packages that support very high current densities and bandwidth requirements. These high performance devices also require a steady and consistent supply of power which becomes challenging as device functionality increases. In addition, there are yield and reliability concerns that arise from the larger package sizes and very fine pitch interconnection that is required to produce higher I/O densities. fcCuBE technology significantly reduces the substrate layer count and complexity, achieving a thinner, lower cost package with high power integrity, superior control over thermal performance and higher resistance to EM over standard flip chip packages.

Package Design

Several body sizes starting from as small as 14X14mm to as large as 35X35mm packages were selected to run various legs in the design of experiments (DOE) at various stages. A wide range of die sizes along with various Si nodes from several foundries were used for the DOE. Table 1 describes the DOE detail in the study. Substrate type and technology is another important parameter to design a lower cost and higher performance package. In this study both plated through hole (PTH) and build up substrates with multilayer counts and lower coefficient of thermal expansion (CTE) core materials were used to meet package performance requirements.

Lower CTE substrate core material was also chosen to control the package warpage/coplanarity in addition to extreme low-K (ELK) die protection. The gap between the bump to nearest trace is the key for the fcCuBE® design. Some of the designs have traces between the bumps. Too narrow of a gap can cause assembly related issues such as solder bridging, shorting, etc. In these designs we have as low as a 15um gap between the bump to the nearest trace.

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package type	body size (mm)	die size (mm)	Si node	bump pitch (um)	# traces between the bumps	bump dia (um)	bump height (um)
fcBGA-H	14X14	9X10	28	120	1	56	58
fcBGA-H	17X17	9X10	28	120	1	56	58
fcBGA	19X19	7X8	28	110	2	64	70
fcBGA-H	23X23	9X9	28	135			65
fcBGA	25X25	7X8	28	110	2	64	70
fcBGA-H	27X27	11x10	90	80	0	60	63
fcBGA-H	31X31	10X10	28	125	1	66	70
fcBGA-H	35X35	13X13	45	125	1	60	70

Table 1: Fine pitch Cu Pillar fcBGA DOE

The bumping process included polyimide (PI) re-passivation, Ti/Cu under bump metallization (UBM), and Cu pillar plating with a SnAg solder cap on top. Most of the consumer application has multiple rows of peripheral bumps at a very fine bump pitch for the I/O while much wider bump pitches are in the die center area. Figure 1 shows the fcCuBE® Cu bump and SnAg solder cap along with BOL trace detail for a given bump pitch design. Overall Cu pillar and solder cap height were optimized in order to create the optimum stand-off height required for successful flow of capillary underfill (CUF) process in the assembly.

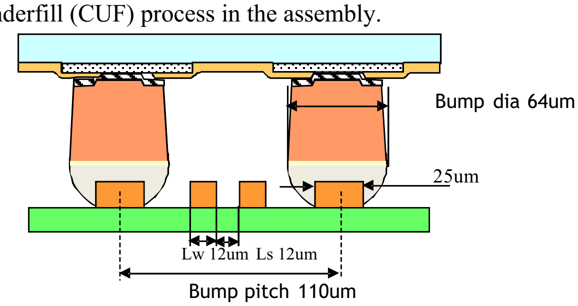

Figure 1: Bump pattern, and Cu pillar bump dimension detail w/ BOL pad

Assembly Process

The assembly process included several design iterations for bump height in order to optimize the CUF flow underneath the die. Too short of bump standoff design can result in CUF voids for larger die size. Too tall of bump can cause ELK crack in the die. Initially a design with very tall Cu pillar (55um pillar height with 30um cap) was chosen which enables a significant gap height increase. Higher pillar over solder cap ratio increased die level stress, resulting in ELK crack (white bump) during the chip attach process. Significant ELK damage was experienced with a taller pillar design even though it gives a better CUF process in the design. Figure 2 below shows white bump with taller pillar height with the actual product.

Extensive simulation has been conducted to understand the safe limit of pillar/solder cap ratio. Finally, a design with smaller pillar and around 30um solder cap with full open solder resist (SR) was introduced which maintained a smaller bump height to address the white bump issue.

The detailed assembly process, including flip chip attach, flux cleaning, underfilling, lid or heat spreader attach, solder ball mounting, marking, etc, was fully optimized for assembly. Figure 3 shows the typical assembly process flow for a standard lidded flip chip BGA package. The critical areas in the assembly process were identified as chip attach, underfilling and ball mount processes.

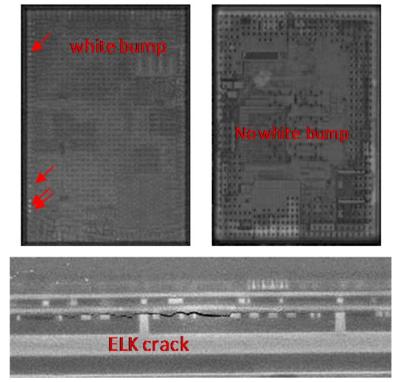

Figure 2: white bump w/ taller bump (left picture), and no white bump w/ smaller bump (right picture)

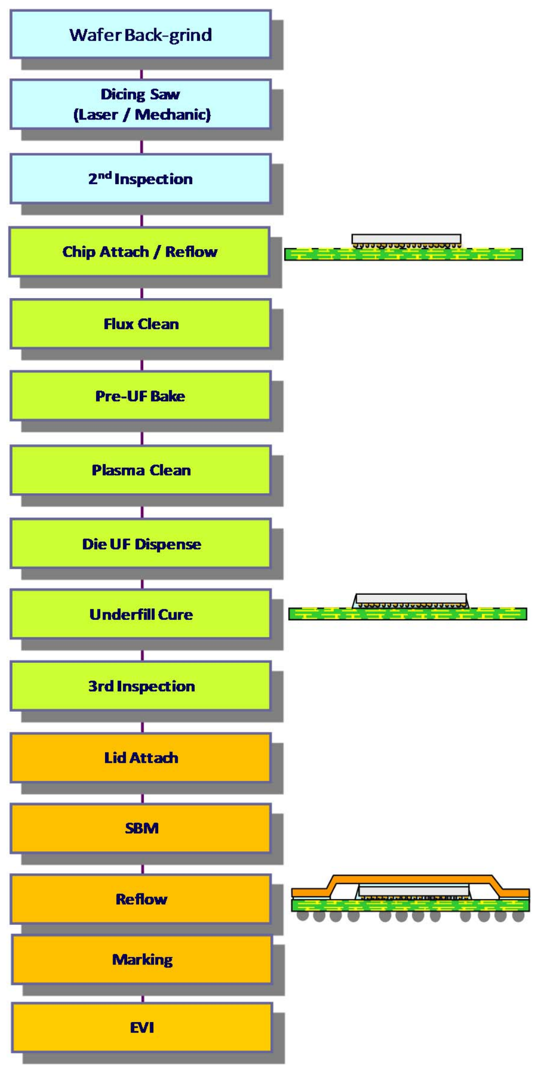

Figure 3: Typical assembly flow for standard flip chip BGA (fcBGA) package

Additionally, an optimum amount of flux is needed in the chip attach process to make a good joint for very fine size/pitch Cu pillar. Die placement also plays a crucial role. If by any means the die are misaligned, solder bridging, non-wet, etc. might occur in the chip attach process. Another important concern is white bump (bump delamination) for low K/ELK die. The white bump risk is much lower with the BOL pad versus bond on pad (BOP) interconnect. Having a smaller BOL pad helps to resolve the die level stress during the chip attach process by shifting the stress from die side to substrate side.

The effect of die thickness on the die or extreme low K (ELK) was throughly investigated for fine pitch Cu pillar interconnection. Typically, Cu pillar bump is much stiffer than standard Pb free bump. High stiffness Cu pillar bump creates excessive die stress due to CTE mismatch during the chip attach process in assembly. Standard 300mm wafers come with 780um die thickness. A much higher propensity of ELK delamination or white bump occurs in thick die compared to thin die. In this study both 780um and 500um thin die were used to carry out the DOE. Hammer test or multi reflow test were conducted at 260^0C peak for non-underfilled packages in order to verify the ELK silicon robustness. With full thickness Si (780um), lots of white bumps were encounterd right after chip attach process reflow whereas for thin die (500um thickness), configuration first ELK crack was observed after 20X reflow. The effect of bump diameter and solder resist opneing (SRO) size was also investigated in the study. The results in Table 2 captured various effects on the white bump from the multiple reflow test. Failure parts were cross-sectioned comprehensively to look at the failure mode and intensity of the ELK crack as shown in Figure 4 below.

Die thickness	Bump diameter	Substrate SRO	White bump results @ 260'C multi reflow				
			T=0	5x	10x	20x	30x
780um	56um	bigger	5/10	5/10	8/10	10/10	10/10
780um	56um	smaller	2/10	4/10	5/10	10/10	10/10
780um	60um	bigger	0/10	0/10	1/10	1/10	8/10
780um	60um	smaller	0/10	0/10	0/10	1/10	10/10
500um	60um	bigger	0/10	0/10	0/10	0/10	2/10
500um	60um	smaller	0/10	0/10	0/10	0/10	0/10
500um	56um	bigger	0/10	0/10	0/10	2/10	7/10
500um	56um	smaller	0/10	0/10	0/10	4/10	5/10

Table 2: White bump results for non-underfilled packages after various level of multi reflow tests

Fine tuning of the DOE was completed with optimum die thickness, bump diameter, and SRO size. No anomalies were found in the die or interconnections. Finally, a quick temperature cycle (QTC) at -40^0 to 60^0C was conducted to verify the DOE. No ELK crack or white bump found from the verification DOE as shown in Table 3 below. Optimum design parameters were selected for final package qualification.

Materials Choices

Package warpage is a big concern for flip chip BGA packages with medium to large die and body size with thin core susbtrates. A low CTE core substrate is required for large packages with ELK die. Low CTE cores help mitigate "white bump" issues and reduce warpage by minimizing thermal mismatch between the substrate and die. In this study, 4-6L of build up substrates with thin and thick core low CTE materials were used The substrate was designed with proper metal balance on each layer to minimize warpage and other potential substrate related failures in the package. Several iterations of the design and assembly process were performed to finalize the process window.

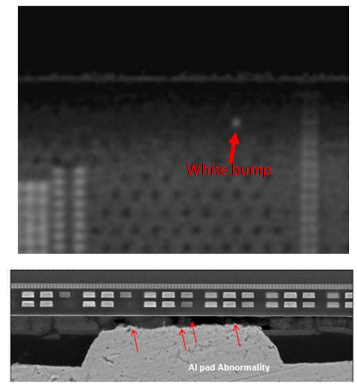

Figure 4: White bump scanning picture and bump cross-section after 20X reflow

Die thickness	Bump diameter	Substrate SRO	White bump results @ QTC (-40~60'C)			
			T=0	15x	30x	50x
500um	60um	small	0/10	0/10	0/10	0/10
			0/10	0/10	0/10	0/10
			0/10	0/10	0/10	0/10

Table 3: No white bump after QTC 50X

Our empirical data from the DOE shows package warpage or coplanrity was not much of a concern due to flip chip packages which are built mostly with a heatspreader or lid and die size was not very large. Thermo Moir'e data in Figure 5 shows a 35X35mm flip chip package with 4L build up substrate package warpage at various temperatures was well below the requirement (150um at 25^0C).

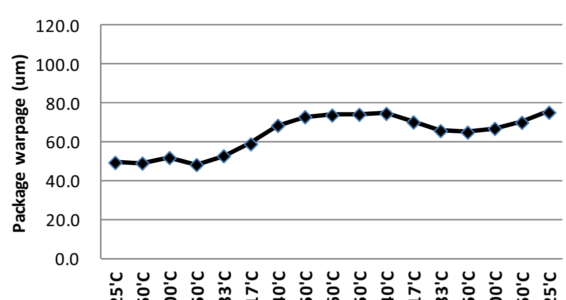

Figure 5: Package warpage at various temperatures for 35X35mm fcBGA-H with 4L low CTE core substrate

Selecting the right underfill material for flip chip packages is always challenging. A large die package requires high Tg (glass transition temperature) underfill to protect the bumps from CTE mismatch. On the other hand, high Tg underfill creates more die or ELK stress in the assembly process. It is a tradeoff between die or ELK stress and bump protection.

Moreover, high Tg underfill will create high package warpage or coplanarity. In this study a moderate Tg underfill was selected to fulfill the package needs. A combination of “I” and “U” pass dispense was used to make sure no underfill voids, underfill bleed out or creeping.

A typical spiral dispense pattern on the die backside with supplier recommended cure profile was applied in the assembly process shown in Figure 6 below. A silicone gel based with high thermal conductivity soft thermal interface material (TIM) was selected in the DOE. The standard process was followed to detect TIM and adhesive coverage in the assembly process. Lid pull tests were performed after end of line (EOL) for all legs to make sure lids were attached properly and maintained a certain adhesion strength. Both TIM and lid adhesive materials were extensively characterized to meet certain requirements such as a wider process window to dispense epoxy and attach lid, higher lid-pull strength, low thermal resistance, etc

A check list for various process steps was monitored during the assembly process to ensure it met all required conditions. The detailed check list with monitoring methodologies is shown in Table 4.

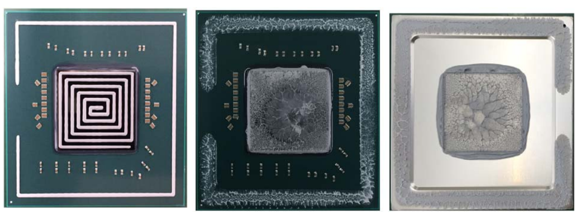

Figure 6: Typical TIM and adhesive dispense pattern

Electrical open short (O/S) tests were performed after each accelerated test condition even for characterization DOE builds. Any failed units were cross-sectioned to verify failure results and failure mode. Learning from the characterization builds was fanned out to subsequent builds including qualification build.

Process	Check Point /Methodology	Check Items
DP	Visual / optical Inspection	Sawing quality, Die chipping, Kerf width, Wafer Crack, solder void, bump shear
SPP/CCM	Visual Inspection	Paste wetting, Mis-placement, Tombstoning
FCA	Die peel	Flux Residue, coverage, Bump Joint
	X-ray	Alignment, Bridge, Cold Joint, Bump Void
UF	Visual Inspection	UF Bleed-out, Fillet Height/Coverage Creeping on die, UF crack
	C-SAM	Void, Delam, Bump/IMC/Pre-solder crack
LDA	Visual Inspection	Placement Accuracy, Bleed-out, BLT
	Lid pull	Adhesive strength
	C-SAM	TIM/Adhesive void, coverage
SBM	Ball Shear	Ball Shear Strength
	X-ray	Solder ball void
BE/EVI	AOI POD compliance	Coplanarity, Dimension, construction analysis, HT Warpage
Reliability Test	C-SAM / X-section	Delamination / white bump / bump & pre-solder crack

Table 4: Checklist for assembly and reliability

Qualification Build

The leg with the best result from the characterization build was selected for both package and board level qualification. Packages were built with 3 different lots each with 77 units. No noticeable issues were encountered in the package assembly process. C-mode scanning acoustic microscope (CSAM) results was taken on every part after the underfill cure process to make sure no underfill voids or delamination occurred in the packages. A robust process, bill of materials (BOM), and carrier/fixtures were selected for the entire development and qualification build to make sure no anomaly such as solder bridging, non-wet, underfill delamination, or solder crack occurred in the package with fcCuBE® technology. Some of the packages in the development had a really narrow bump pitch for mass reflow process which was very challenging for the chip attach process. One of the DOE legs had 80um pitch in line bumps. A comprehensive DOE was carried out to optimize the process and BOM for 80um bump pitch package. Figure 7 shows a bump cross-section data of 80um bump pitch Cu pillar package after various reliability tests.

Package level post reliability requirements were kept the same in the qualification build (JEDEC standard package level reliability tests: preconditioning with MSL-4, uHAST, HTS, and TCB). The detailed test matrix with sample size for the package level qualification for one given body size build is shown in Table 5. Again, electrical open short tests were performed on every part after every read-point. No failure or other degradation was observed in any of the qualification build samples. Table 5 shows complete reliability data of qualification build parts.

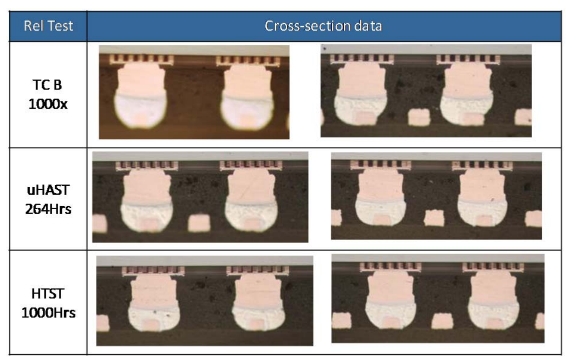

Figure 7: Reliability data for 80um bump pitch fcCuBE® with fcBGA

Pre-con	Reliability Test							
	uHAST		TC "B"			HTST (w/o precon)		
	96hrs	168hrs	200x	500x	1000x	168hrs	500hrs	1000hrs
0/308 (No Fail)	0/77 (No Fail)	0/77 (No Fail)	0/231 (No Fail)	0/231 (No Fail)	0/231 (No Fail)	0/77 (No Fail)	0/77 (No Fail)	0/77 (No Fail)

Table 5: Qualificaiton build reliability data for a 31X31mm fcBGA-H with fcCuBE®

Extensive failure analyses were conducted on post reliability parts to see bump crack or bump shape on BOL pad or other oddities in the package. A cross-section was done on a few parts after each reliability test. Figure 8 shows a sampling of bump images after uHAST, HTS, and TCB tests for 31X31mm fcBGA.

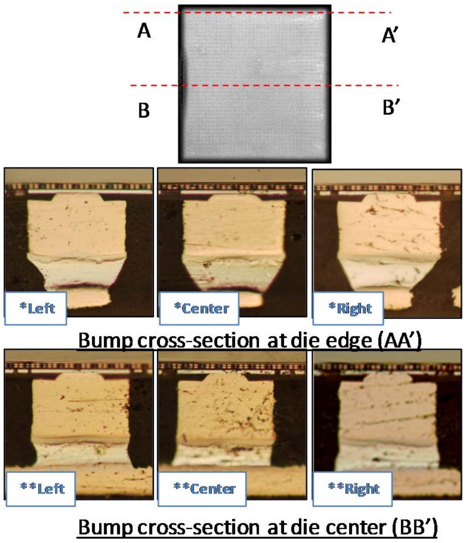

Figure 8: Bump cross-section data after reliability tests.

Board Level Reliability (BLR) and Electromigration (EM) data

Lots of work on BOL or fcCuBE® with fcCSP package showed exceptionally good BLR and EM reliability data irrespective of bump pitch. Equivalent or even better BLR results are expected due to more optimized BOM, and processes are used in the fcBGA packages.

EM tests were performed on fine pitch Cu pillar BOL interconnections and standard bond on pad (BOP) structure for various temperature and current conditions. Over 7000 hours of EM test were conducted and no failures were observed. Very insignificant resistance shifts were observed irrespective of current stress and temperatures [1]. BOL EM data proved that the technology is much more robust for fine pitch high performance packages for consumer or other flip chip applications.

Cost Impact

With the phenomenal expansion of flip chip technology offering and manufacturing footprint, assembly suppliers are positioning themselves to support the strategic growth of very cost effective high performance flip chip for consumer and other applications. One of the major cost components of flip chip package is the substrate. With the evolution of new BOL technology, significant cost benefit can be achieved from the substrate side. Due to finer pitch bump the die size can be reduced significantly for a given I/O package. Consumer applications such as set top box, digital TV, industrial, and automotive products are also migrating to high power with higher density and some special requirements. As the cost of product development continues to grow, assembly supplier investments for product line technology grows at the same rate. Time-to-market pressures remain high, with design cycles getting shorter and market-driven product requirements skyrocketing with much cheaper prices. This is one of the key challenges across the assembly suppliers. By using such BOL technology in the flip chip package and other value engineering (VE) driven technologies, the need for low cost high performance fine pitch flip chip packages is expected to grow significantly for next generation advanced packages.

fcCuBE® technology can enable lower costs for the product through proper and extensive co-design with the Silicon. Cu column with BOL can provide the increased I/O density for advanced Si nodes through pitch reduction. fcCuBE technology has the capability of driving bump pitches down to 80um or even less. This can enable a significant amount of die shrin,k especially for advanced silicon nodes while managing the requirements for similar or even higher I/O count for the silicon. Thus, a product can utilize the performance improvement from an advanced silicon node and still be able to manage I/O density and I/O count requirements for the Silicon and resulting die size. In some instances, fcCuBE® can even drive up to 30% die shrink for the advanced silicon node and maintain the same I/O count. This has a tremendous impact on the cost because not only does it drive packaging cost but also can drive a lower silicon cost, thereby enabling an overall lower cost of the product.

From a purely packaging cost perspective, the two main areas of cost reduction come from the reduction in substrate layer count and elimination of Pre-solder or solder on Pad (SOP) process during substrate manufacturing.

For a multi-layer fcBGA package, fcCuBE® can drive a reduction in the number of substrate layers needed to route the I/O signals for fine pitch Cu pillar design. Several routing studies have demonstrated that fcCuBE® can route a 6 layer substrate design using lead free solder bump and solder on Pad, to a 4 layer substrate using fcCuBE® technology. This provides a significant cost reduction for the packaging component of the product cost.

In a lead free solder interconnect, the substrate suppliers typically add pre-solder on the substrate pad to enable the interconnect formation with the lead free solder bump on the silicon die. The cost of pre-solder can be significant depending on number of I/Os and bump pitch. fcCuBE® technology eliminates the need for pre-solder (SOP) on the substrate pad as the Cu pillar with lead free solder cap directly attaches to the substrate metal pad to make the interconnection.

Conclusions

Continuous trends in bump pitch reduction, performance improvement and Si node reduction, and the resultant move to ELK dielectrics, have created the need for a robust flip chip bump process that is serviced by the copper pillar technology. The fine pitch fcCuBE® technology evaluation for low cost consumer package has proved that the technology is very robust for assembly and performs exceptionally well through all critical JEDEC level reliability, and high current EM testing. The technology currently is in high volume production for fcBGA and has excellent assembly yield and dppm level losses for opens/shorts.

Furthermore, the fcCuBE® technology now is extending beyond consumer markets as the SoCs undergo various application environments, including rigorous automotive qualification program.

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References

[1] Nokibul Islam et al, "Electromigration for Advanced Cu Interconnect and the Challenges with Reduced Pitch Bumps" *Electronic Components and Technology Conference, 2014. ECTC 2014. 64th,* Lake Buena Vista, Fl, May 27th-30th, 2014

[2] John Savic et al, "Mixed Pitch BGA (mpBGA) Packaging Development for High Bandwidth-High Speed Networking Devices" *Electronic Components and Technology Conference, 2012. ECTC 2012. 62nd,* San Diego, CA, pp. 450-456, May 29th-June 1st, 2012

[3] Hamid Eslampour et al, "Low Cost Cu Pillar fcPOP Technology", *Electronic Components and Technology Conference, 2012. ECTC 2012. 62nd,* San Diego, CA, pp. 871-876, May 29th-June 1st, 2012

[4] US Patent Nos. 7368817, 7700407, 7901983, 7973406, 8076232 and 8188598. Bump-on-lead Flip Chip Interconnection, Raj Pendse, Nov. 2004

[5] JH Yoo et al, "Analysis of Electromigration for Cu Pillar Bump in Flip Chip Package", *Electronics Packaging Technology Conference, 2010. EPTC 2010. 12th,* Singapore, pp. 129-133, December 8-10th, 2010.

[6] Joshi, M. et al, CuBoL (Cu Pillar on BoL) Technology: A Low Cost Flip Chip Solution Scalable to High IO Density, Fine Bump Pitch and Advanced Si Node. Proc 61st Electronic Components and Technology Conf, FL, May 2011.

[7] Eslampour, H. et al, Next Generation PoP Technology, Advanced Interconnect Technologies, IMAPS Conference, July 13, 2011.

[8] Pendse R, et al, "Low Cost Flip Chip (LCFC): An Innovative Approach for Breakthrough Reduction in Flip Chip Package Cost", 60th Electronic Components and Technology Conf, Las Vegas, Ca, June 2010.

[9] Eric Oyuang, et al, "Improvement of ELK Reliability in Flip Chip Packages using Bond-on-Lead (BOL) Interconnect Structure", IMAPS Conference, October 2010.

[10] Pendse R., et al, "Bond-on-Lead: A Novel Flip Chip Interconnection Technology for Fine Effective Pitch and High I/O Density", Proc 56th Electronic Components and Technology Conf, San Diego, Ca, May. 2006. pp. 16-23